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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/814,714 | 03/23/2001 | Satoshi Kamiya | 017446/0310 | 4370 |

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| EXAMINER | |
|---|---|
| RYMAN, DANIEL J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2665 | |

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/814,714 | KAMIYA, SATOSHI | |
| | Examiner | Art Unit | |
| | Daniel J. Ryman | 2665 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 8/4/2005 have been fully considered but they are not persuasive. On pages 7-9 of the Response, Applicant asserts that "Hanaki does not disclose determining time slots for performing specific recited tasks, information transfer processing and reservation processing." In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Although Hanaki does not expressly disclose the tasks of information transfer processing and reservation processing, Hanaki is not required to show these tasks since Applicant has disclosed these tasks as prior art (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page 8, line 17-page 10, line 14). Therefore, Examiner maintains that the combination of Applicant's admitted prior art and Hanaki discloses determining time slots for performing specific recited tasks, information transfer processing and reservation processing.

2. Applicant further asserts that Hanaki does not disclose "assigning time slots of the same size for these specific tasks." Examiner, respectfully, disagrees. In Hanaki, each task is allotted an equal amount of time in which to finish (time for IF cycle is the same as for the ID cycle, EX cycle, etc.) (Fig. 2). Such a requirement is necessary in pipeline processing where one stage cannot pass its processed information to the next stage until the next stage is also finished processing. Therefore, the transfer of information from one stage to the next, in a pipeline processor, is limited by the length of time required by the stage having the longest processing

time. As such, Examiner maintains that Hanaki discloses assigning time slots of the same size for the different tasks.

3. In view of the foregoing, Examiner maintains that the claims are obvious in view of the cited prior art.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Chao et al. (USPN 5,724,351) in further view of Hanaki (USPN 6,269,439).

3. Regarding claim 1, Applicant admits as prior art a distributed pipeline scheduling method for a system which includes a plurality of input ports for inputting data (Fig. 8 and page 1, line 14-page 4, line 21), a plurality of output ports for outputting data (Fig. 8 and page 1, line 14-page 4, line 21), a data switch element for switching the data input from the input ports and transferring the data to the output ports (Fig. 8 and page 1, line 14-page 4, line 21), and a scheduler having a distributed scheduling architecture for controlling the data switch element (Figs. 8 and 9 and page 1, line 14-page 5, line 24), and determines connection reservations between the input ports and the output ports (Figs. 8 and 9 and page 1, line 14-page 5, line 24), comprising the steps of: causing the scheduler to assign time slots to information transfer processing and reservation processing (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and

page 8, line 17-page 10, line 14); and processing information transfer processing and reservation processing in the assigned time slots (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page 8, line 17-page 10, line 14).

Applicant does not admit as prior art causing the scheduler to independently assign time slots of the same size to information transfer processing and reservation processing, respectively; and processing information transfer processing and reservation processing in the assigned time slots in a pipeline fashion. Rather Applicant admits as prior art that the scheduler assigns the same time slot to information transfer processing and reservation processing (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page 8, line 17-page 10, line 14). Chao teaches, in a packet switching system, that adequate performance of a large switch is only possible by using pipeline techniques in the scheduler (arbiter) (col. 6, lines 27-37); however, Chao does not specify how the pipeline processing is performed. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to process information transfer processing and reservation processing in assigned time slots in a pipeline fashion in order to have adequate performance in a large switch.

Applicant in view of Chao does not expressly disclose that the scheduler independently assigns time slots of the same size to information transfer processing and reservation processing, respectively; however, Applicant in view of Chao does disclose performing pipeline processing in the scheduler (Chao: col. 6, lines 27-37) where the scheduler performs information transfer processing and reservation processing (AAPA: Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page 8, line 17-page 10, line 14). Hanaki teaches, in a pipeline processing system, independently assigning time slots of the same size (time for IF cycle is the same as for the ID

cycle, EX cycle, etc.) to different stages of the pipeline processor in order to increase the amount of processing that can be accomplished per unit time compared to a processor without pipeline processing (Fig. 2 and col. 1, lines 42-67). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to independently assign time slots of the same size to information transfer processing and reservation processing, respectively, in order to increase the amount of processing that can be accomplished per unit time compared to a processor without pipeline processing.

4. Regarding claim 2, Applicant in view of Chao in further view of Hanaki discloses that the scheduler includes N (N is a natural number) distributed scheduling modules for performing information transfer processing and reservation processing in units of time slots (AAPA: Figs. 8 and 9 and page 1, line 14-page 5, line 24), and the step of processing comprises the step of determining a connection reservation, by using the distributed scheduling module, for a predetermined time slot at a time point after a lapse of a time corresponding to a number time slots from a time slot from which the reservation processing is started (AAPA: Figs. 8 and 9 and page 1, line 14-page 5, line 24; Chao: col. 6, lines 27-37; and Hanaki: Fig. 2 and col. 1, lines 42-67). Applicant in view of Chao in further view of Hanaki does not expressly disclose that the number of time slots is 2N-1 time slots; however, Applicant in view of Chao in further view of Hanaki does disclose that there is a number of time slots between the start of the processing and the predetermined time slot which is being reserved (AAPA: Figs. 8 and 9 and page 1, line 14-page 5, line 24; Chao: col. 6, lines 27-37; and Hanaki: Fig. 2 and col. 1, lines 42-67). It is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular

recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Since Applicant in view of Chao in further view of Hanaki discloses that there is a number of time slots between the start of the processing and the predetermined time slot which is being reserved, it would have been obvious at the time of the invention to use any number of time slots, including 2N-1, absent a showing of criticality by Applicant.

5. Regarding claim 3, Applicant admits as prior art a distributed pipeline scheduling system comprising a plurality of input ports for inputting data (Fig. 8 and page 1, line 14-page 4, line 21), a plurality of output ports for outputting data (Fig. 8 and page 1, line 14-page 4, line 21), a data switch element for switching the data input from the input ports and transferring the data to the output ports (Fig. 8 and page 1, line 14-page 4, line 21), and a scheduler having a distributed scheduling architecture for controlling the data switch element (Figs. 8 and 9 and page 1, line 14-page 5, line 24), wherein said scheduler comprises a plurality of input modules for performing reservation processing for different time slots (Figs. 8, 9, and 13; page 1, line 14-page 10, line 14), and said input modules respectively comprise information transfer processing means and reservation processing means for performing information transfer and reservation processing for different time slots (Figs. 8, 9, and 13; page 1, line 14-page 10, line 14).

Applicant does not admit as prior art that the scheduler comprises a plurality of input modules for performing reservation processing for different time slots at the same time in a

pipeline fashion, and the input modules respectively comprise information transfer processing means and reservation processing means for performing information transfer and reservation processing for different time slots at the same time in a pipeline fashion. Chao teaches, in a packet switching system, that adequate performance of a large switch is only possible by using pipeline techniques in the scheduler (arbiter) (col. 6, lines 27-37); however, Chao does not specify how the pipeline processing is performed. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the scheduler comprise a plurality of input modules for performing reservation processing in a pipeline fashion and to have the input modules respectively comprise information transfer processing means and reservation processing means for performing information transfer and reservation processing in a pipeline fashion in order to have adequate performance in a large switch.

Applicant in view of Chao does not expressly disclose that that the scheduler comprises a plurality of input modules for performing reservation processing for different time slots at the same time, and said input modules respectively comprise information transfer processing means and reservation processing means for performing information transfer and reservation processing for different time slots at the same time, wherein the different time slots are of the same size and wherein information transfer processing and reservation processing are respectively performed in the different time slots of the same size; however, Applicant in view of Chao does disclose performing pipeline processing in the scheduler (Chao: col. 6, lines 27-37) where the scheduler performs information transfer processing and reservation processing (AAPA: Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page 8, line 17-page 10, line 14). Hanaki teaches, in a pipeline processing system, independently assigning time slots to different stages of the pipeline

processor in order to increase the amount of processing that can be accomplished per unit time compared to a processor without pipeline processing wherein the different time slots are of the same size (time for IF cycle is the same as for the ID cycle, EX cycle, etc.) and wherein each stage are respectively performed in the different time slots of the same size (Fig. 2 and col. 1, lines 42-67). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the scheduler comprise a plurality of input modules for performing reservation processing for different time slots at the same time in a pipeline fashion, and said input modules respectively comprise information transfer processing means and reservation processing means for performing information transfer and reservation processing for different time slots at the same time in a pipeline fashion wherein the different time slots are of the same size and wherein information transfer processing and reservation processing are respectively performed in the different time slots of the same size in order to increase the amount of processing that can be accomplished per unit time compared to a processor without pipeline processing.

6. Regarding claim 4, Applicant admits as prior art a distributed scheduler for distributed pipeline scheduling which is used by a packet switch in a packet switching system (Fig. 8 and page 1, line 14-page 4, line 21), comprising: a plurality of input modules respectively having output port reservation information receiving sections, allocators, and output port reservation information transmitting sections and serving to perform distributed scheduling (Figs. 8, 9, and 13 and page 1, line 14-page 10, line 14), wherein said output port reservation information receiving sections, allocators, and output port reservation information transmitting sections

execute processing for different reservation time slots (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page 8, line 17-page 10, line 14).

Applicant does not admit as prior art that the output port reservation information receiving sections, allocators, and output port reservation information transmitting sections within each input module simultaneously execute processing for different reservation time slots. Chao teaches, in a packet switching system, that adequate performance of a large switch is only possible by using pipeline techniques in the scheduler (arbiter) (col. 6, lines 27-37); however, Chao does not specify how the pipeline processing is performed. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform pipeline processing in each input module in order to have adequate performance in a large switch.

Applicant in view of Chao does not expressly disclose that the output port reservation information receiving sections, allocators, and output port reservation information transmitting sections within each input module simultaneously execute processing for different reservation time slots, wherein the processing comprises information transfer processing and reservation processing performed, respectively, in time slots of the same size. Hanaki teaches, in a pipeline processing system, simultaneously execute processing for different items in the elements of a pipeline processor in order to increase the amount of processing that can be accomplished per unit time compared to a processor without pipeline processing, wherein the processing comprises processing of each stage in time slots of the same size (time for IF cycle is the same as for the ID cycle, EX cycle, etc.) (Fig. 2 and col. 1, lines 42-67). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the output port reservation information receiving sections, allocators, and output port reservation information transmitting

sections within each input module simultaneously execute processing for different reservation time slots, wherein the processing comprises information transfer processing and reservation processing performed, respectively, in time slots of the same size, in order to increase the amount of processing that can be accomplished per unit time compared to a processor without pipeline processing.

7. Regarding claims 5-7, Applicant in view of Chao in further view of Hanaki implicitly discloses that the time slots of the same size are determined as being the largest among (a) time for information transfer reception and information expansion, (b) time for reservation processing, and (c) time for format conversion and information transfer transmission (Hanaki: Fig. 2 and col. 1, lines 42-67) where, since one stage cannot pass its processed information to the next stage until the next stage is completed, the length of the time slot/cycle for each stage to complete processing is determined by the longest processing time required by a stage in a pipeline.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jordan et al. (USPN 5,805,849) see col. 1, lines 52-67 which pertain to the benefits of pipelined processors. Kumar (USPN 6,122,274) see entire document which pertains to a decentralized pipeline control for a switch.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 7:00-4:30 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel J. Ryman
Examiner
Art Unit 2665

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